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Att'y Docket No. 003921.00011

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent of:

Terry Lee GOODE

U.S. Pat. App. No.: 09/841,974

Filing Date: April 24, 2001

For: EMULATOR WITH SWITCHING NETWORK
CONNECTIONS

Examiner: Fred O. Ferris, III

Group Art Unit: 2128

INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
Alexandria, Virginia 22313-1450

Sir:

Pursuant to his duty of disclosure under 37 C.F.R. §1.56, Applicant brings the documents listed in the attached PTO-1449 form to the attention of the Examiner in the above-identified patent application.

In accordance with the Notice published in the Official Gazette of August 5, 2003, Applicant has not provided copies of the U.S. patents and published U.S. patent applications listed in the attached PTO-1449. A copy of each of the listed foreign patent documents and non-patent literature, however, is attached hereto.

A first Official Action issued for this application on November 9, 2004. Accordingly, the Commissioner is authorized to charge the fee required under 37 C.F.R. §1.97(c)(2) to Deposit Account No. 19-0733. Applicant therefore submits that this Information Disclosure Statement is being timely presented in accordance with 37 C.F.R. §1.97(c).

While Applicant is presenting the documents listed in the attached PTO-1449 form, Applicant does not waive any right to take appropriate action to establish patentability over the listed documents should one or more of these documents be applied as a reference against any claim in this application.

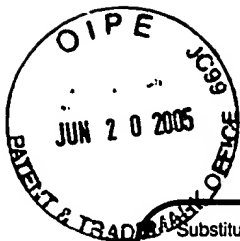
Applicant respectfully asks that the documents listed on the attached PTO-1449 form be considered by the Examiner and made officially of record, and that a listing of the same appear on the face of any patent which may issue from this application.

Respectfully submitted,

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PTO/SB/08a (08-03)



PTO/SB/08b(08-03)

Approved for use through 07/31/2006. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

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Substitute for form 1449B/PTO

**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**

(Use as many sheets as necessary)

Sheet 2 of 2

Complete if Known

| | |
|------------------------|--------------------|
| Application Number | 09/841,974 |
| Filing Date | 4/24/01 |
| First Named Inventor | Terry Lee Goode |
| Art Unit | 2128 |
| Examiner Name | Fred O. Ferris III |
| Attorney Docket Number | 003921.00011 |

NON PATENT LITERATURE DOCUMENTS

| Examiner Initials * | Cite No. ¹ | Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published. | T ² |
|------------------------|--------------------------|--|----------------|
| | | Kronstadt, et al., "Software Support for the Yorktown Simulation Engine," 19 th Design Automation Conference, Paper 7.3, 1982, pp. 60-64 | |
| | | Koike, et al., "HAL: A High-Speed Logic Simulation Machine," IEEE Design & Test, Oct. 1985, pp. 61-73 | |
| | | Shear, "Tools Help you Retain the Advantages of Using Breadboards in Gate-Array Design," EDN, Mar. 18, 1987, pp. 81-88 | |
| | | J.W. Babb, "Virtual Wires: Overcoming Pin Limitations in FPGA-based Logic Emulation," Masters Thesis, Massachusetts Institute of Technology, Department of Electrical Engineering and Computer Science, Nov. 1993; Also available as MIT/LCS Technical Report TR-686 | |
| | | M. Dahl, J. Babb, R. Tessier, S. Hanono, D. Hoki, and A. Agarwal, "Emulation of the Sparcle Microprocessor with the MIT Virtual Wires Emulation System," IEEE Workshop on FPGAs for Custom Computing Machines '94 (FCCM '94), Apr. 1994 | |
| | | R. Tessier, J. Babb, M. Dahl, D. Hanono and A. Agarwal, "The Virtual Wires Emulation System: A Gate-Efficient ASIC Prototyping Environment," ACM Workshop on FPGAs (FPGA '94), Feb. 1994 | |
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| | | IKOS Systems to Acquire Virtual Machine Works; IKOS Systems Mar. 11, 1996 | |
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| | | Feng, "A Survey of Interconnection Networks," Computer, Dec. 1981, pp. 12-27 | |
| | | Chapter 36, "Switching Networks and Traffic Concepts," Reference Data for Radio Engineers, Howard W. Sams & Co., 1981, pp. 36-1 to 36-16 | |
| | | S. Hanono, "Inner View Hardware Debugger: A Logic Analysis Tool for the Virtual Wires Emulation System," Masters Thesis, MIT Department of Electrical Engineering and Computer Science, Jan. 1995; Also available as MIT/LCS Technical Report. | |

Examiner
SignatureDate
Considered

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

¹ Applicant's unique citation designation number (optional). ² Applicant is to place a check mark here if English language Translation is attached.

This collection of information is required by 37 CFR 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 120 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450. If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.